WHAT IS CLAIMED IS:

1. A processing apparatus comprising:

an internal circuit including a CPU executing programs, at least one internal circuit having a predetermined function and a bus line connecting said CPU to said internal device, extending externally and transferring an address and data; and

an external circuit provided externally of an externally extending portion of said bus line and including at least one external device having a predetermined function, wherein

said internal circuit includes a ciphering section interposed at an entrance to an external side and ciphering the address and the data on the bus line by ciphering patterns according to a plurality of regions divided from an address space allotted to entirety of said at least one external device.

2. A processing apparatus according to claim 1, wherein

the ciphering patterns adopted by said ciphering section include one ciphering pattern in which neither the address nor data is ciphered.

3. An processing apparatus according to claim 1, wherein

said external circuit includes a plurality of external devices; and

said ciphering section performs ciphering using ciphering patterns according to said plurality of external devices, respectively.

4. A processing apparatus according to claim 1, wherein

said ciphering section outputs a dummy address and dummy data to the externally extending portion of said bus line at

timing at which said external circuit is not accessed.

5. A processing apparatus according to claim 1, wherein said CPU is supplied with a clock and executes the programs synchronously with the supplied clock, and said ciphering section is supplied with a clock and performs ciphering synchronously with the supplied clock; and

a clock supply section for supplying a clock at a higher speed than a speed of the clock supplied to said CPU, to said ciphering section.

6. A processing apparatus according to claim 1, comprising:

ciphering pattern determination means for recognizing a constitution of said external circuit and determining a ciphering pattern of said ciphering section according to the constitution of said external circuit.

7. A processing apparatus according to claim 1, wherein said ciphering section ciphers the address and the data on said bus line by ciphering patterns according to the plurality of regions divided from the address space allotted to the entirety of said no less than one external device and according to application programs executed by said CPU.

8. A processing apparatus according to claim 1, comprising:

a deciphering section connected to the externally extending portion of said bus line, and returning the ciphered address and the data on the bus line to an address and data which are not ciphered.

9. A processing apparatus according to claim 1, comprising:

ciphering pattern change means for changing a ciphering pattern whenever a predetermined initialization operation is carried out for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device.

10. A processing apparatus according to claim 1, wherein

said ciphering section adopts a ciphering pattern in which ciphered data is changed according to the address, for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device, to thereby cipher the data.

11. A processing apparatus comprising:

an internal circuit including a CPU executing programs, at least one internal device having a predetermined function, and a bus line connecting said CPU to said internal device, extending externally and transferring an address and data; and

an external circuit provided externally of the externally extending portion of said bus line, and storing information, wherein

said internal circuit has information rewrite means for ciphering and rewriting at least part of the information stored in said memory in a predetermined initial operation.

12. A processing apparatus according to claim 11, wherein

said predetermined initialization operation is an

initialization operation when the apparatus is first powered on.

13. A processing apparatus according to claim 11, wherein

said information rewrite means generates a random number, and performs ciphering by adopting a ciphering pattern using the generated random number.

14. A processing apparatus according to claim 11, wherein

the at least part of the information stored in said memory has been already ciphered before said predetermined initialization operation is carried out; and

said information rewrite means temporarily returns the at least part of the information to information which is not ciphered, and rewrites the information by ciphering again the information by adopting a different ciphering pattern.

15. A processing apparatus according to claim 14, wherein

deciphering information for returning said at least part of information to information before being ciphered is stored in said memory; and

said information rewrite means temporarily returns the at least part of information to the information before being ciphered using the deciphering information.

16. A processing apparatus according to claim 14, wherein

said at least part of information is ciphered by a public

key, and a secret key is embedded in this processing apparatus; and

said information rewrite means temporarily returns the at least part of information to the information before being ciphered using the secret key.

17. A processing apparatus according to claim 14, wherein

said processing apparatus comprises an information acquisition section for acquiring ciphered deciphering information to return said at least part of information to the information before being ciphered; and

said information rewrite means deciphers the ciphered deciphering information acquired by said information acquisition section, fetches deciphering information in plain text, and temporarily returns the at least part of information to the information before being ciphered using this deciphering information in plain text.

18. A processing apparatus according to claim 1, wherein

said internal circuit holds a ciphering pattern adopted by said ciphering section;

the processing apparatus further comprises a tamper detection section detecting tamper; and

ciphering pattern destruction means for destroying the ciphering pattern held in said internal circuit in response to tamper detection made by said tamper detection section.

19. A processing apparatus according to claim 11,

wherein

said internal circuit holds a ciphering pattern adopted by said ciphering section;

the processing apparatus further comprises a tamper detection section detecting tamper; and

ciphering pattern destruction means for destroying the ciphering pattern held in said internal circuit in response to tamper detection made by said tamper detection section.

20. An integrated circuit constituted by mounting:

a CPU executing programs; at least one internal device having a predetermined function; a bus line connecting said CPU to said internal device, externally extending, at least one external device having a predetermined function provided externally of the externally extending portion of the bus line, and transferring an address and data; and

a ciphering section interposed at an entrance to an external side, and ciphering the address and the data on the bus line by ciphering patterns according to a plurality of regions divided from a space allotted to entirety of the at least one external device provided externally of the externally extending portion of the bus line.

21. An integrated circuit according to claim 20, wherein

the ciphering patterns adopted by the ciphering section include one ciphering pattern in which neither the address nor data is ciphered.

22. An integrated circuit according to claim 20,

wherein

in case where a plurality of external devices are provided externally of the externally extending portion of said bus line, said ciphering section performs ciphering by the ciphering patterns according to said plurality of external devices, respectively.

23. An integrated circuit according to claim 20, wherein

said ciphering section outputs a dummy address and dummy data to the externally extending portion of said bus line at timing at which said external circuit is not accessed.

24. An integrated circuit according to claim 20, wherein

said CPU is supplied with a clock and executes the programs synchronously with the supplied clock, and said ciphering section is supplied with a clock and conducts ciphering synchronously with the supplied clock; and

said ciphering section operates with a clock at a higher speed than a speed of the clock with which said CPU operates.

25. An integrated circuit according to claim 20, comprising:

ciphering pattern determination means for recognizing a constitution of said external circuit, and for determining a ciphering pattern of said ciphering section according to the constitution.

26. An integrated circuit according to claim 20, wherein

said ciphering section ciphers the address and the data on said bus line by ciphering patterns according to the plurality of regions divided from the address space allotted to the entirety of said no less than one external device and according to application programs executed by said CPU.

27. An integrated circuit according to claim 20, comprising:

ciphering pattern change means for changing a ciphering pattern whenever a predetermined initialization operation is performed, for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device.

28. An integrated circuit according to claim 20, wherein

said ciphering section ciphers the data by adopting a ciphering pattern in which ciphered data is changed according to the address, for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device.

29. An integrated circuit by comprising:

a CPU executing programs;

at least one internal device having a predetermined function; and

a bus line connecting said CPU to said internal device, extending externally, a memory storing information provided externally of an externally extending portion of the bus line, and transferring an address and data; wherein

the integrated circuit includes information rewrite means for ciphering and rewriting at least part of the information stored in said memory in a predetermined initialization operation.

30. An integrated circuit according to claim 29, wherein

said predetermined initialization operation is an initialization operation when the apparatus is first powered on.

31. An integrated circuit according to claim 29, wherein

said information rewrite means generates a random number, adopts a ciphering pattern using the generated random number and thereby performs ciphering.

32. An integrated circuit according to claim 29, wherein

at least part of the information stored in said memory has been already ciphered before said predetermined initialization operation is carried out; and

said information rewrite means temporarily returns the at least part of the information to information which is not ciphered, and rewrites the information by ciphering again the information by adopting a different ciphering pattern.

33. An integrated circuit according to claim 32, wherein

deciphering information for returning said at least part of information to information before being ciphered is stored

in the memory; and

said information rewrite means temporarily returns said at least part of information to the information before being ciphered using the deciphering information.

34. An integrated circuit according to claim 32, wherein

said at least part of information is ciphered by a public key, and a secret key is embedded in this processing apparatus; and

said information rewrite means temporarily returns the at least part of information to the information before being ciphered using the secret key.

35. An integrated circuit according to claim 32, wherein

said processing apparatus comprises an information acquisition section for acquiring ciphered deciphering information to return the at least part of information to the information before being ciphered may be provided; and

said information rewrite means deciphers the ciphered deciphering information acquired by said information acquisition section, fetches deciphering information in plain text, and temporarily returns the at least part of information to the information before being ciphered using this deciphering information in plain text.